

Fig. 1

Fig. 2A

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Bus with multiple masters (and slaves):-

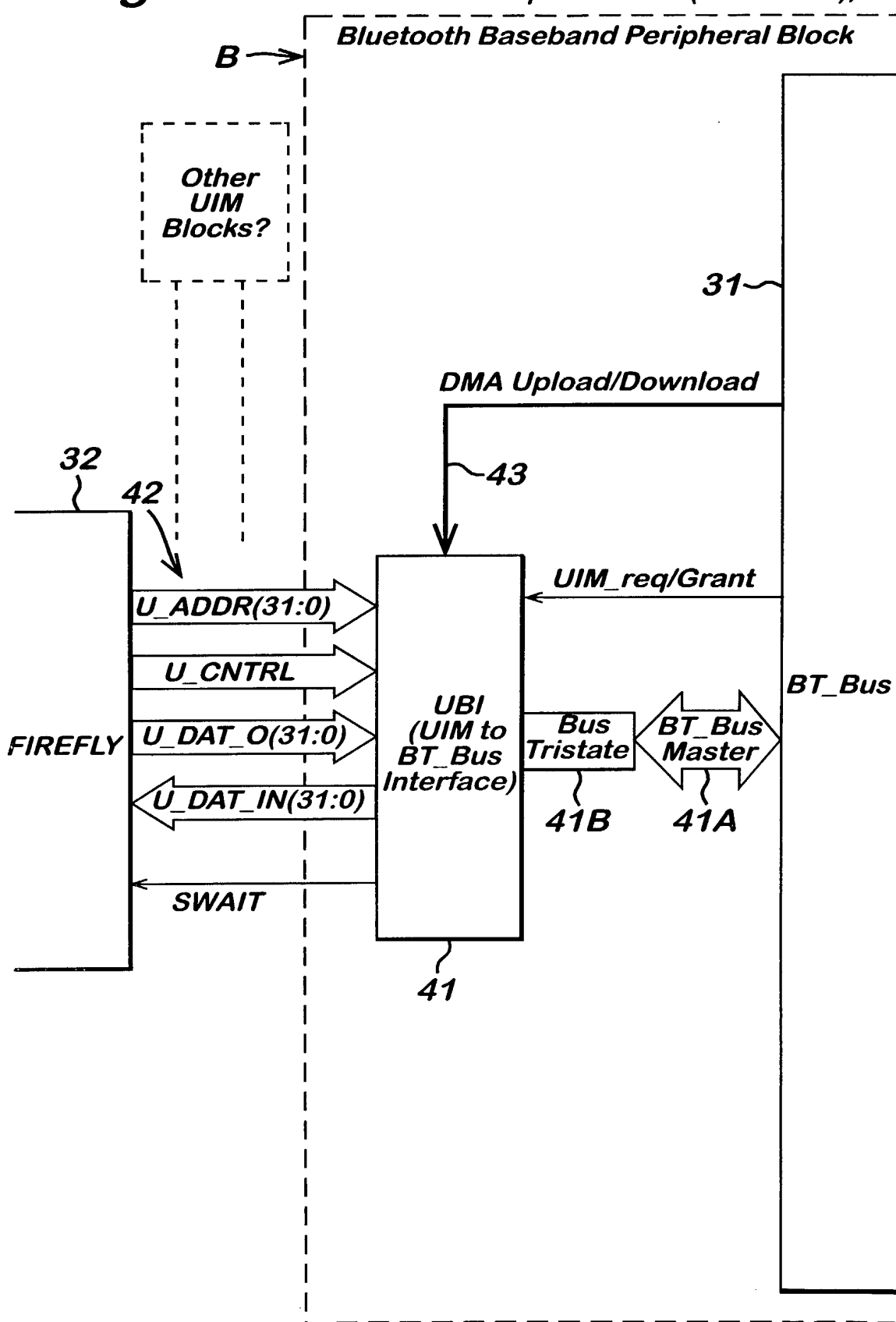


Fig. 2B

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B

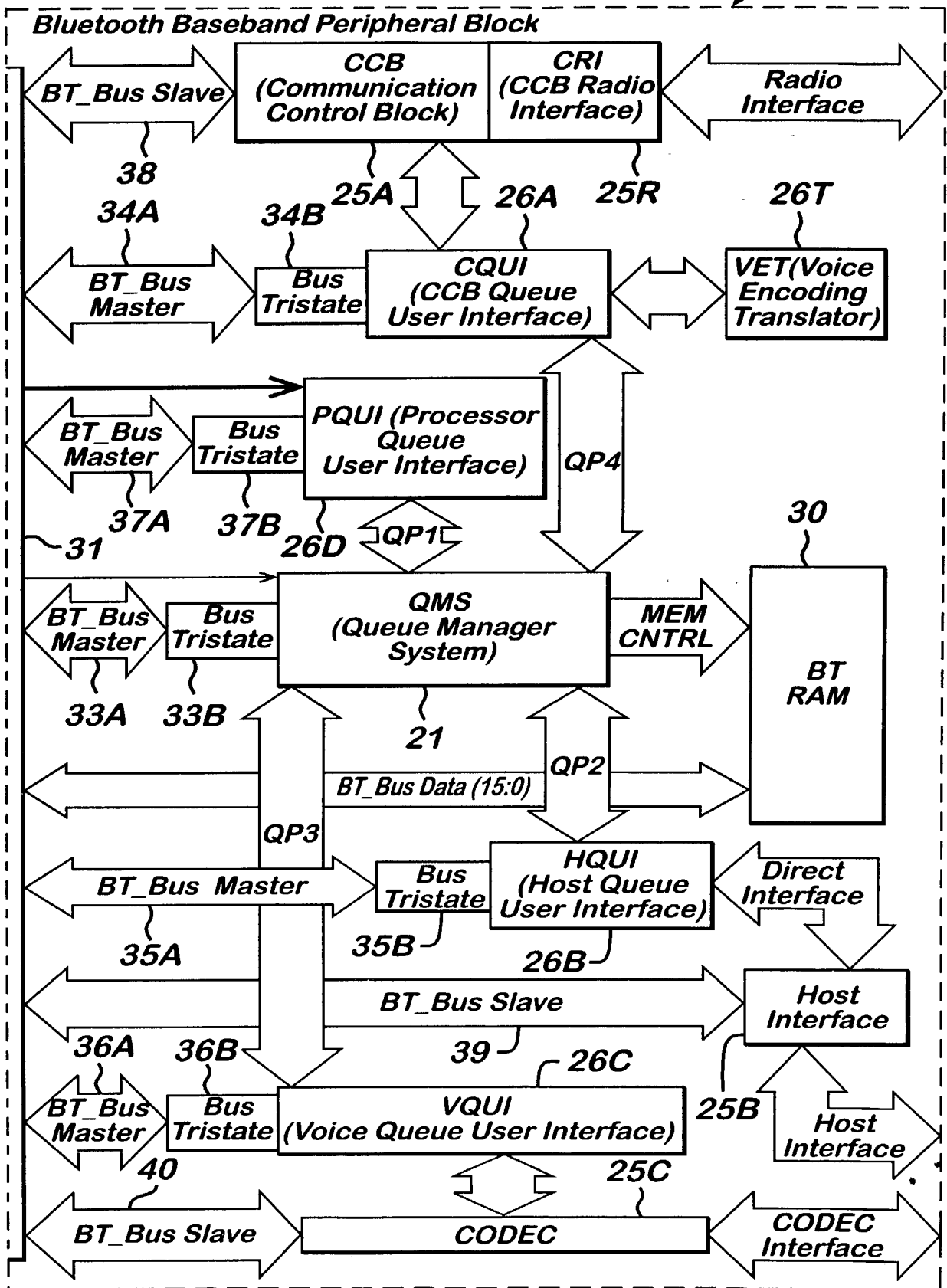
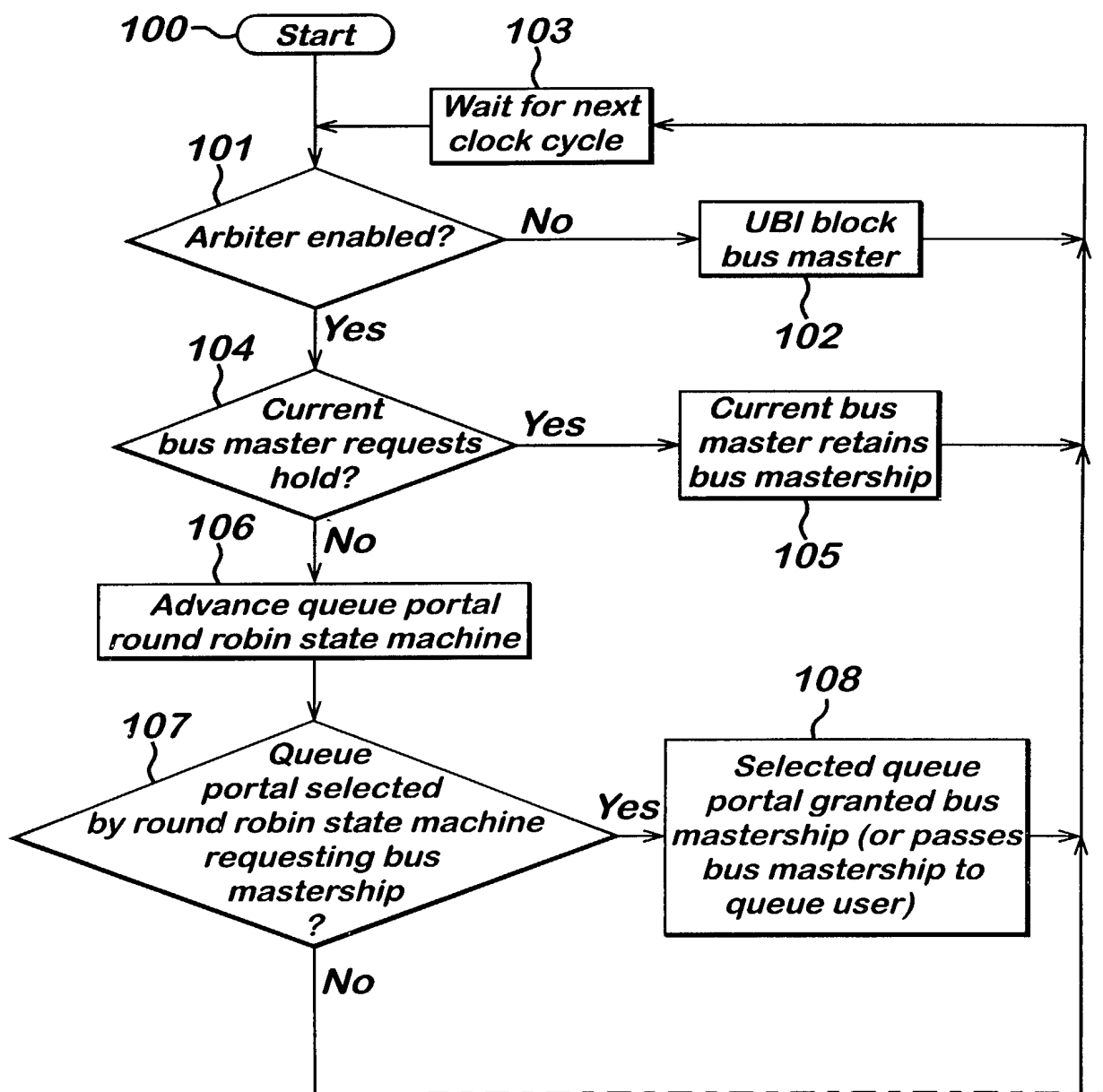


Fig. 3A Arbiter state machine

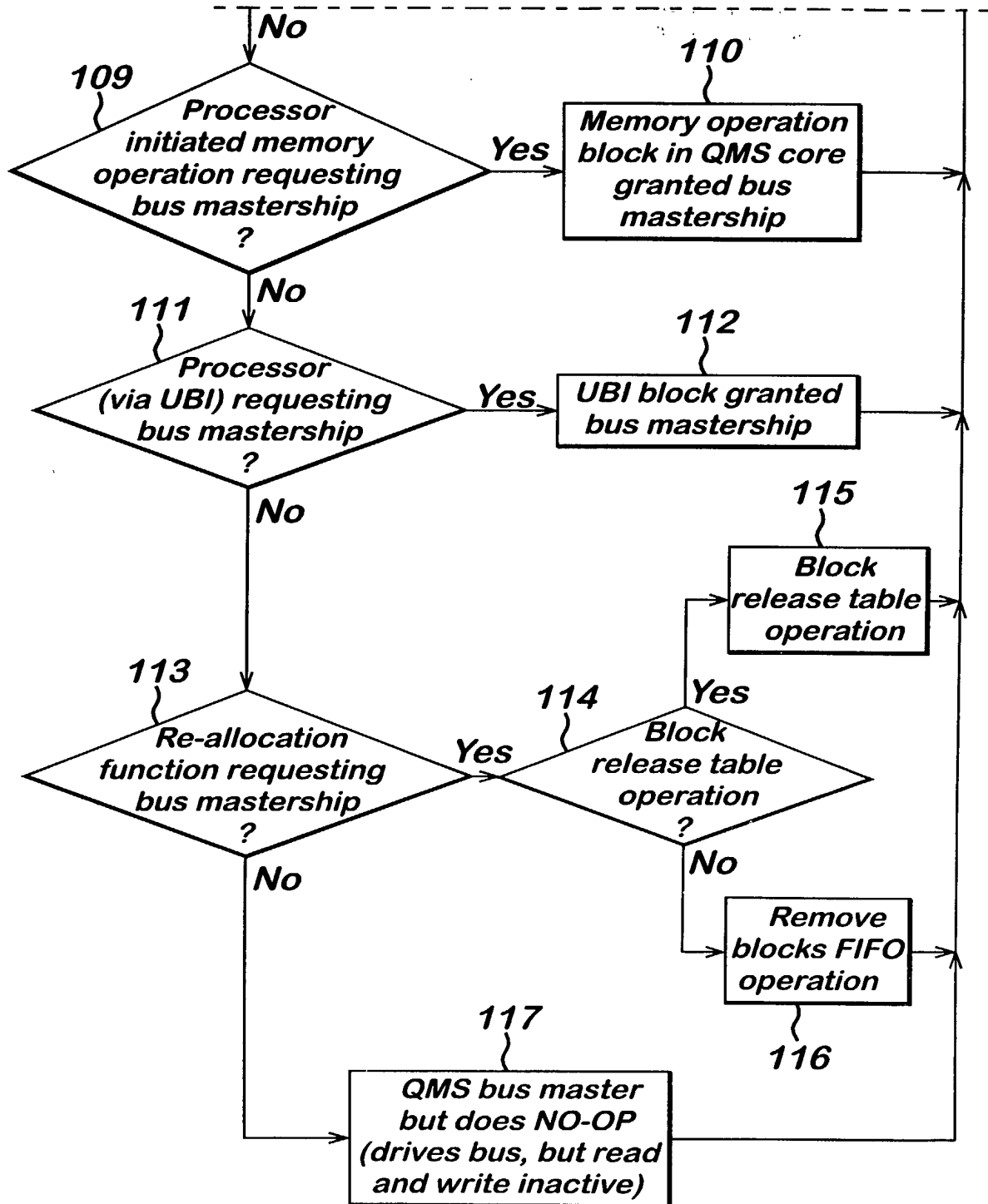


Fig. 3B